Application No. 10/814,774

Attorney Docket No.: 02453.0033.NPUS00

In the Claims:

(Currently Amended) A processor readable medium [storing]encoding a
data structure for supporting one or more packet modification operations, the data
structure comprising:

a pointer to a sequence of one or more commands, for execution by a processor, implementing one or more packet modification operations and stored in a first memory area; and

a pointer to a burst of one or more data or mask items for use by the processor in executing the one or more commands stored in a second memory area distinct from the first.

- (Original) The processor readable medium of claim 1 wherein the first and second memory areas are located in different memories.
- (Original) The processor readable medium of claim 1 wherein the first and second memory areas are located in the same memory.
- (Original) The processor readable medium of claim 1 wherein the one or more commands are stored in a packed format.
- (Original) The processor readable medium of claim 1 wherein the one or more data or mask items are stored in a packed format.
- (Original) The processor readable medium of claim 1 wherein the one or more data or mask items comprise data items and associated mask items, with a data item stored adjacent to its associated mask item.
- (Original) The processor readable medium of claim 1 wherein the first and second memory areas are located in a memory implemented off chip from a modification processor configured to execute the one or more commands.
- (Original) The processor readable medium of claim 1 wherein the first memory area is located in a memory implemented on chip with the modification processor.

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 (Original) The processor readable medium of claim 1 wherein the data structure comprises one or more pointers, each to a sequence of one or more commands implementing one or more packet modification operations.

- (Original) The processor readable medium of claim 9 wherein the data structure comprises one or more pointers, each to a burst of one or more data or mask items.
- 11. (Currently Amended) A method of performing one or more packet modification operations on a packet while located within a first portion of a switch, the packet including a data structure index previously added while the packet was located within a second portion of the switch, the method comprising:

retrieving from a memory a data structure corresponding to the data structure index, and comprising a pointer to a sequence of one or more commands, for execution by a processor, implementing one or more packet modification operations and stored in a first memory area, and a pointer to a burst of one or more data or mask items for use by the processor in executing the one or more commands stored in a second memory area distinct from the first;

retrieving from the first memory area the one or more commands;

retrieving from the second memory area the one or more data or mask items for use by the one or more commands; and

executing the one or more commands by the processor, thereby performing one or more packet modification operations on the packet.

- (Original) The method of claim 11 wherein the first portion of the switch is an egress portion of the switch.
- (Original) The method of claim 11 wherein the second portion of the switch is an ingress portion of the switch.
- (Original) The method of claim 12 wherein the first and second memory areas are located in different memories.

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 (Original) The method of claim 12 wherein the first and second memory areas are located in the same memory.

- (Original) The method of claim 12 wherein the one or more commands are stored in a packed format.
- 17. (Original) The method of claim 12 wherein the one or more data or mask items are stored in a packed format.
- 18. (Original) The method of claim 12 wherein the one or more data or mask items comprise data items and associated mask items, with a data item stored adjacent to its associated mask item.
- 19. (Original) The method of claim 12 wherein the first and second memory areas are located in a memory implemented off chip from a modification processor which executes the one or more commands.
- (Original) The method of claim 12 wherein the first memory area is located in a memory implemented on chip with the modification processor.
- 21. (Original) The method of claim 12 wherein the data structure comprises one or more pointers, each to a sequence of one or more commands implementing one or more packet modification operations.
- 22. (Original) The method of claim 12 wherein the data structure comprises one or more pointers, each to a burst of one or more data or mask items.
- 23. (Currently Amended) A method of performing one or more packet modification operations on a packet while located within a first portion of a switch, the packet including a data structure index previously added while the packet was located in a second portion of the switch, the method comprising:
 - a step for retrieving from a memory a data structure corresponding to the data structure index, and comprising a pointer to a sequence of one or more commands, for execution by a processor, implementing one or more packet modification operations and stored in first memory area, and a pointer to a burst

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of one or more data or mask items for use by the processor in executing the one or more commands stored in a second memory area distinct from the first;

- a step for retrieving from the first memory area the one or more commands;
- a step for retrieving from the second memory area the one or more data or mask items for use by the one or more commands; and
- a step for executing the one or more commands by the processor, thereby performing one or more packet modification operations on the packet.